REMARKS/ARGUMENTS

Claims 1-30 stand rejected in the outstanding Official Action. Applicant has amended claims 1, 4, 8, 23 and 30 and therefore claims 1-30 remain in this application.

The Examiner's acknowledgment of Applicant's claim for foreign priority and receipt of the certified copies of the priority documents is very much appreciated. Additionally, the Examiner's indication of PTO acceptance of the previously filed formal drawings is appreciated. Finally, the Examiner's consideration and acknowledgment of Applicant's previously submitted Information Disclosure Statement is appreciated.

On page 2 of the outstanding Official Action, the Examiner objects to the previously submitted abstract which included a reference to Figure 8. The reference to Figure 8 has been cancelled in the above amendment to the abstract, thereby obviating any further objection thereto.

Claims 4, 8 and 23 stand objected to because of various informalities. Claim 4 was objected to as failing to include antecedent basis for the term "said busy signal" in line 2. Applicant appreciates the Examiner's suggestion, but has realized that claim 4 should have been dependent from claim 3 which provides proper antecedent basis for "busy signal." The change in dependency has been made in this Amendment.

With respect to claims 8 and 23, the Examiner correctly noted that the word "to" appears to be missing in these claims. Applicant has amended claims 8 and 23 to correct this error.

Finally, Applicant has noticed that claim 30 recited "apparatus as claimed in claim 29" when in fact claim 29 was a method claim. Applicant has amended claim 30 to reference "method as claimed in claim 29."

In view of the above amendments, claims 4, 8, 23 and 30 are believed to comply with all PTO formality requirements and any further objection thereto is respectfully traversed.

Claims 1, 2, 5, 8-10, 12-17, 20, 23-25 and 27-30 stand rejected under 35 USC §103 as unpatentable over Noble (U.S. Patent 5,760,636) in view of Clark (U.S. Patent 6,425,086). Applicant's independent claims 1 and 16 recite an apparatus and method which involves processing data. Applicant has amended claim 1 to more positively recite structural features of Applicant's claimed processing circuit, i.e., the circuit includes a processing mode "for performing data processing operations" and a holding mode "for holding state without performing data processing operations." Applicant's apparatus comprises the processing circuit and the power supply and clock signal control circuit as specified in the claim.

Applicant's specification, beginning on page 2, line 16 and extending over through page 3, line 6, discloses the desirability to reduce energy consumption of data processing systems in general, while at the same time being able to increase their performance level to deal with increasingly computationally intensive tasks. As Applicant notes, "such tasks often require highly intensive processing operations for short periods of time followed by relatively long idle times in which little computation is required."

The conventional approach to varying performance levels is to adjust both the clock cycle as well as the voltage applied in order to adjust the performance of the processor. While systems could have an infinite number of clock frequencies and applied voltages, a two step system is taught in the Noble reference. Noble operates at two different clock frequencies and operating voltages and teaches transitioning from normal operation to a low power operation and transitioning back from a low power operation to a normal operation. During the first transition

(to a low power operation), the clock frequency is first lowered and then the voltage is lowered. During the second transition, from a low power mode, the voltage is first raised and then the clock frequency is raised.

While it is appreciated that the Examiner believes that the low power mode of Noble is the equivalent of Applicant's claimed "holding mode," it is clear that Applicant's independent claims 1 and 16 specify that Applicant's holding mode requires the stoppage of the clock signal. In other words, the clock signal is not just reduced; it is stopped. This is not the case in the Noble reference wherein the low power mode is such that the processor continues to operate, although at a lower frequency (see Noble, column 2, lines 56-65). Thus, not only does Noble not disclose Applicant's claimed invention, Noble suggests that the low power setting requires the processor to continue operating. Thus, the Noble reference clearly would lead one of ordinary skill in the art **away** from Applicant's claimed invention.

On page 4 of the Official Action, the Examiner admits that "Noble fails to disclose in a holding mode to hold state without performing processing operations when said power supply has a holding configuration and said clock is stopped." This admission is very much appreciated and confirms Applicant's analysis above.

The Examiner also admits Noble fails to disclose "a target rate signal indicative of a target rate of data processing operations to be performed by said processing circuit" and this admission is also appreciated. However, at lines 5-7 on page 4 of the Official Action, the Examiner has enclosed a portion of Applicant's claim 1 language in parentheses and has added his own comments, i.e., "(to modulate a target rate mode control signal to switch said processing circuits between said processing mode and said holding mode – addressed above and added here

for clarity) so as to achieve said target rate." Applicant's actual claim language has no parenthetical expressions and the target rate signal serves to "switch said processing circuits between said processing mode and said holding mode."

In other words, Applicant reads the above admission as the Examiner appreciating that Noble, because it does not teach any "holding mode," cannot teach a target rate signal which causes the system to switch between processing mode and holding mode because it does not even have the claimed "holding mode." While Applicant believes he has properly interpreted the Examiner's comments, confirmation and/or clarification as to the admissions relating to the Noble reference is respectfully requested.

Applicant also believes that the Examiner is citing the Clark reference as allegedly teaching control between a data processing mode and a "sleep" mode which the Examiner contends is analogous to the claimed "holding state mode." This contention is respectfully traversed, as the Clark reference actually teaches a "sleep mode" which is entered before adjusting the operating voltage (see Clark, column 5, line 55 to column 6, line 2). The disclosed "sleep mode" is substantially different from the claimed "holding mode."

The present invention uses the "holding mode" in an entirely different way from Clark by switching backwards and forwards between the "processing mode" and the "holding mode" in order to achieve the desired overall processor duty cycle. It can be seen that operating in "processing mode" for 50% of the time and operating in "holding mode" for 50% of the time will provide the data processor with 50% operation. If the processor is desired to operate at 75% of its maximum speed, it would operate in processing mode 75% of the time and holding mode

25% of the time, with the processor alternating back and forth between the two modes so as to achieve the desired 75% duty cycle.

Thus, Applicant's invention permits an infinite variation in duty cycles for its processing circuit, while only having to design the system for a single clock cycle frequency and a single operating voltage. The infinite number of processing frequencies are achievable by modulating the amount of time spent in processing mode and in holding mode. The processing system only has to be designed to operate in two modes (essentially "on" and "off") and not the infinite number of clock cycle frequencies and operating voltages which would otherwise be necessary.

The Clark reference teaching of a "sleep mode" only has the clock stop during the data processor's sleep mode. However, Clark teaches that "relative to clock speed, for example, this [change from and to "sleep" mode] may in some cases be a time consuming operation." Additionally, Clark defines "sleep mode" as comprising "**finishing current operations**, stopping the internal clocks, and stopping the microprocessor phase locked loop (PLL) or similar circuit." (emphasis added, Column 5, lines 61-64). The requirement of "finishing current operations" is not consistent with the claimed "holding mode" or alternating between "processing mode" and "holding mode."

Contrary to the Clark teaching, Applicant's claimed invention requires switching between processing mode and holding mode in order "to achieve said target rate," i.e., the desired operational frequency. (See the last two lines of Applicant's independent claim 1). Clark, on the other hand, teaches only a single data processing operation and a separate sleep mode which takes a relatively long time in terms of clock speed to enter and recover from. Clark does not suggest using the sleep mode in order to adjust the effective operating frequency of the Clark

processor and this would not be possible due to the delays in changing to or from the "sleep mode."

Because neither the Noble nor Clark reference contain any suggestion of switching between a processing mode and a holding mode so as to achieve a variable and desired target rate (operating frequency), even if these two references were combined, they would not render obvious the subject matter of independent claims 1 and 16. Moreover, there is no "reason" or "motivation" identified as to why one of ordinary skill in the art would seek to combine the Noble and Clark references.

Only the Noble reference has any relation to variable operating frequency, and this reference actually teaches away from Applicant's claimed invention because it requires data processor operation during the low power mode – the direct opposite of Applicant's claimed invention. The Clark reference would lead one of ordinary skill in the art away from Applicant's claimed invention as well, because it teaches a sleep mode which takes a relatively long time to enter and recover from. Those of ordinary skill in the art would be clearly aware that this would not be a usable feature in order to obtain the benefit of Applicant's invention, i.e., an infinitely variable processing speed by using varying combinations of processing mode and holding mode.

Inasmuch as independent claims 1 and 16 are not taught by either Noble or Clark, that there is no reason or motivation to combine Noble and Clark, and that both Noble and Clark would lead one of ordinary skill in the art away from Applicant's claimed combination, the combination of these two references does not render obvious the subject matter of the independent claims. Because all claims 2-15 and 17-30 depend from independent claims 1 and

16, respectively, there is no basis for rejecting any other claims over the Noble/Clark combination and any further rejection thereunder is respectfully traversed.

Claims 11 and 26 stand rejected under 35 USC §103 over the Noble/Clark combination and further in view of Kusaka (U.S. Patent 4,823,309). Because claims 11 and 26 depend from claims 1 and 16, respectively, the above comments distinguishing the Noble and Clark combination from claims 1 and 16 are herein incorporated by reference.

Because the Examiner does not indicate how or where the Kusaka reference either teaches or suggests the structure or method steps missing in claims 1 and 16, respectively, even if Kusaka were combined with Noble and Clark, the combination would not disclose Applicant's claimed invention and therefore any further rejection thereunder is respectfully traversed.

Claims 3, 4, 6, 7, 18, 19, 21 and 22 stand rejected under 35 USC §103 over the Noble/Clark combination and further in view of Maher (U.S. Patent 6,088,807). Because claims 3, 4, 6, 7, 18, 19, 21 and 22 depend from claims 1 or 16, the above comments distinguishing the Noble and Clark combination from claims 1 and 16 are herein incorporated by reference.

Because the Examiner does not indicate how or where the Maher reference either teaches or suggests the structure or method steps missing in claims 1 and 16, respectively, even if Maher were combined with Noble and Clark, the combination would not disclose Applicant's claimed invention and therefore any further rejection thereunder is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, amended claims 1-30 are believed to be in condition for allowance and notice to that effect is respectfully requested. In the event the Examiner is of the opinion that a brief telephone

or personal interview will facilitate allowance of one or more of these claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100